

Patent claims

1. A digitally controlled oscillator (1) for
generating a correct-phase output signal at a desired
5 frequency, having an input for supplying a digital
input word (100), having an adder (10) for summing the
digital input words (100), having a stable local
oscillator for supplying a clock signal at a constant
frequency, and having a delay circuit (11, 12) which
10 comprises a coarse delay stage (11) having a plurality
of series-connected coarse delay elements (110) and a
fine delay stage (12) having a plurality of series-
connected fine delay elements (120), where the coarse
delay stage (11) and the fine delay stage (12) are
15 designed such that the total delay brought about by the
coarse delay stage (11) and the fine delay stage (12)
is proportioned such that the maximum total delay and
the minimum total delay of the delay circuit (11, 12)
differ by no more than one period of the clock signal,
20 and where the plurality of fine delay elements (120)
corresponds to the delay by one coarse delay element
(110), wherein each coarse delay element (110) and each
fine delay element (120) comprises a dedicated
actuatable selector (110c; 120f; 120k).
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2. The digitally controlled oscillator (1) as claimed
in claim 1, in which the coarse delay element (110)
comprises a delay element (110b) and the selector
(110c), with one input on the selector (110c) in the
30 respective coarse delay element (110) being connected
to the output of the delay element (110b) of the same
coarse delay element (110) and a further input on the
selector (110c) being connected to the output (110d) of
the selector (110c) in the coarse delay element (110)
35 connected immediately downstream.
3. The digitally controlled oscillator (1) as claimed
in either of claims 1 and 2, in which the fine delay

element (120) has a common input (120a) and at least two drivers (120c, 120d) connected to the common input, with a capacitive load (120e) being provided at the output of one of the two drivers (120d), which
5 oscillator also has one input on the selector (120f) connected to the output of the driver (120c) without the capacitive load and a further input on the selector (120f) connected to the output of the driver (120d) with a capacitive load (120e), and which oscillator has
10 the output of the selector (120f) in the respective fine delay element (120) connected to the common input (120a) of the fine delay element (120) connected immediately downstream.

15 4. The digitally controlled oscillator as claimed in either of claims 1 and 2, in which the fine delay element (120) comprises a plurality of drivers (120j) whose inputs are connected to one another to form a common input (120h) and whose outputs are connected to
20 one another to form a common output (120i), in which also the selector (120k) is designed such that the individual drivers may be activated or deactivated, and in which the common output (120i) is connected to the common input (120h) of the fine delay element (120)
25 connected immediately downstream.

5. A digital phase trimming circuit (PLL), having an input clock signal, having a phase comparator (2), having a filter (3), having a digitally controlled
30 oscillator (1), and having a feedback path which feeds back an output signal generated by the digitally controlled oscillator (1) to the phase comparator (2), possibly with frequency multiplication (4) or frequency division, characterized in that the digitally
35 controlled oscillator (1) is designed in accordance with one of the preceding claims.